

Example: Another CMOS Logic Gate Synthesis

Now let's design a gate that realizes this Boolean algebraic expression:

$$Y = (\bar{A} + \bar{B})C$$

Step 1: Design PDN

First, let's rewrite Boolean expression as $\bar{Y} = f(A, B, C)$:

$$Y = (\bar{A} + \bar{B})C$$

$$\bar{Y} = \overline{(\bar{A} + \bar{B})C}$$

$$\bar{Y} = \overline{(\bar{A} + \bar{B})} + \bar{C}$$

$$\bar{Y} = AB + \bar{C}$$

Q: *Yikes! We cannot write this expression explicitly in terms of **uncomplemented** inputs A , B , and C ! The input C appears as \bar{C} in the expression. What do we do **now**?*

A: An easy problem to solve! We can essentially make a substitution of variables:

$$C' = \bar{C}$$

And thus:

$$\bar{Y} = AB + C'$$

Therefore, the inputs to this logic gate should be A, B, and C' (i.e, A, B, and the complement of C).

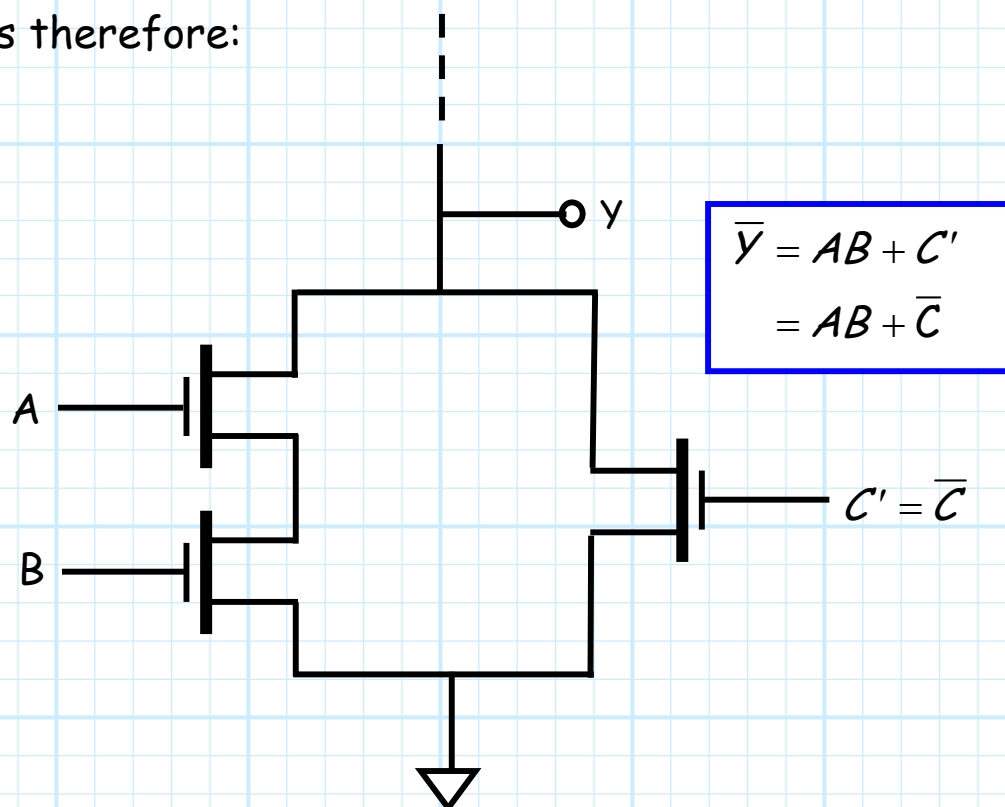
Note that this Boolean expression "says" that:

"The output is low if either, A AND B are both high, OR C' is high"

Of course another way of "saying" this is:

"The output is low if either A AND B are both high, OR C is low"

The PDN is therefore:



Step 2: Design the PUN

Note we have a similar problem as before—the expression for Y **cannot** explicitly be written in terms of complemented inputs \bar{A} , \bar{B} , and \bar{C} :

$$Y = (\bar{A} + \bar{B})C$$

Note we can again solve this problem by using the same substitution of variable C :

$$C' = \bar{C}$$

$$\bar{C}' = C$$

Therefore:

$$\begin{aligned} Y &= (\bar{A} + \bar{B})\bar{C}' \\ &= (\bar{A} + \bar{B})C \end{aligned}$$

This expression “says” that:

“The output will be high if, either A OR B are low, AND C is **low**”

Which is equivalent to saying:

“The output will be high if, either A OR B are low, AND C is **high**”

The CMOS digital logic device is therefore:

